Notes on using Analog Devices' DSP, audio, & video components from the Computer Products Division
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ADSP-21xx Multi-channel Slot Assignments for the AD1847

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Question:

I'm learning to use the EZ KIT Lite board (for the 2181) and I'm confused about the multi-channel operation of the serial port. I understand that the CODEC and 2181 are communicating via the SPORT0 in 32 channel, 2 wire mode. The way I understand the documentation both the transmit and receive functions are operating simultaneously and are each occupying time slots 0,1 and 2 of each 32 slot window.

What confuses me is the actual code that enables the individual channels. In the AD-supplied SPORT0 initialization code:

```
ax0 = b#0000000000000111;   dm
(SPORT0_TX_Channels0) = ax0;

      {   ^15                    00^   transmit word
enables: channel # == bit # }


ax0 = b#0000000000000111;   dm
(SPORT0_TX_Channels1) = ax0;

       {   ^31                   16^   transmit word  enables
}


ax0 = b#0000000000000111;   dm
(SPORT0_RX_Channels0) = ax0;

       {   ^15                   00^   receive word enables  }

ax0 = b#0000000000000111;   dm
(SPORT0_RX_Channels1) = ax0;

       {   ^31                   16^   receive word enables }
```

Apparently , time slots 0,1,2,16,17,and 18 are being enabled. Slots 0,1,2 are for the status, left data and right data words. What are 16,17 and 18 for?

Answer:

The AD1847 supports either 32 (FRS bit=LO) or 16 (FRS bit = HI) bit time slots. The ADSP-21xx SPORT0 can be programmed for either 24 or 32-bit time slots, and we recommend using FRS=LO. The easiest interface design between the ADSP-2181 and the AD1847 is to use the bit states assigned by default after reset with FRS=LO (32 time slots). At reset default the AD1847's frame sync frequency is one half the selected sample frequency with two samples per frame. The reason we developed the code to accept 2 samples per frame sync is to allow the DSP to use up more of the available time slots per frame sync, since time slot allocation on the DSP was selected to meet either the T1 interface standard (24 time slots, Wide Area Networking Protocol) or E1 (32 slots, European Standard for Wide Area Networks).

With the AD1847's FRS bit = 0 (32 slots per frame), slots are paired (0 with 16, 1 with 17, 2 with 18, etc.) Slots 0 and 16 are Control Words for consecutive samples, slots 1 and 17 are Left Playback Data for consecutive samples, and slots 2 and 18 are Right Playback Data for consecutive samples. The reason why we enable channels 16, 17 & 18 is to ensure we will receive valid data from the codec during those time slots, since the codec will be transmitting valid data also for those time slots. Please refer to page 18 of the AD1847 Data Sheet for further discussion on Time Slot Assignments.